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检测
TESTING
CNAS L0095

TEST REPORT

NAME OF SAMPLE: Fixed Flush Socket-outlet

CLIENT: Mordio Electrical Co., Ltd.

CLASSIFICATION OF TEST: Commission Test

CVC Testing Technology Co., Ltd.

MORDIO.COM BEN +8618805875966

Test Report

Name of product: Fixed Flush Socket-outlet	Trade mark: MORDIO
Type/model: K1.1A-041, K1.2-041, K1.22-041, K2-041, K3.0-041, L3.4-041, A1-041, A2-041, A3-041, S1.1-041, K1.23-041, K3.2-041, S1-041, S1.2-041, S1.3-041, S1.4-041, S5.1-041, S3.1-041, S3-041, A4-041, AI-041, S1.5-041, L2-041, S5-041, T1-041, T2-041, T3-041, T3.1-041, T4-041, T8-041	Sample status: --
Manufacturer: Mordio Electrical Co., Ltd.	Commissioned by: Mordio Electrical Co., Ltd.
Manufacturer address: Building 2, No.388, Binhai 13th Rd., Economic And Technological Development Zone, Wenzhou, Zhejiang, China	Commissioner address: Building 2, No.388, Binhai 13th Rd., Economic And Technological Development Zone, Wenzhou, Zhejiang, China
Quantity of sample: 18pcs	Sampled by: —
Sample identification: 18-1~18-18	Sampling at (place): —
Means of receiving: Submitted by Manufacturer	Means of sampling: —
Classification of test: Commission Test	Sampling date: —
Receiving date: 2024-03-26	Date (s) of performance of tests: 2024-08-16
Tested according to: BS EN 62680-1-1:2015	Test item: Full safety test

Test conclusion:

The EUT submitted by Mordio Electrical Co., Ltd. is tested according to BS EN 62680-1-1:2015. All the items tested comply with the requirements of standard.

Test result: Pass.

Seal of CVC

Date of issue:2024-08-15

Approved by: Meng Zhiqiang Reviewed by: Chen Yunhua Tested by: Li Pengzhong

Description and illustration of the sample:

1. The class II structure USB power supply module was tested as a sub assembly according to IEC 62368-1:2018 when incorporated into the socket-outlet to supply for information technology equipment.
2. All models are identical in electrical, mechanical, physical construction except for model number, front panel frame and Material of faceplate. All the tests were performed on model K3.0-041 unless otherwise specified.
3. USB Input: 175-250V～,50/60Hz,350mA
   USB Output: 5V⎓2.1A
4. The maximum ambient temperature is 35℃ declared by the manufacturer.
5. The mains supply tolerance was specified of ±10% by manufacturer.
6. IEC 62680-1-1:2015 equal to BS EN 62680-1-1:2015.

Description of the sampling procedure:

—

Description of deviation from the standard, if any:

—

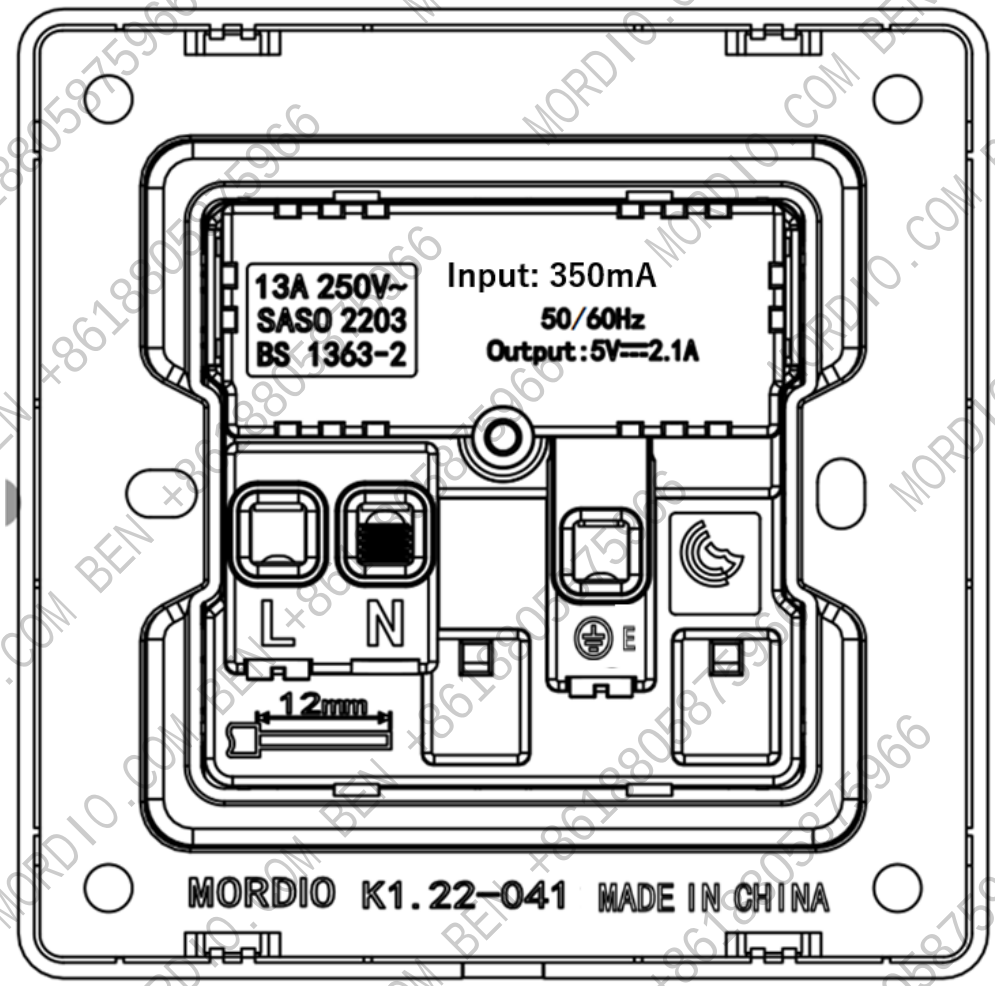
Remarks:

Factory name and address:

Name: Mordio Electrical Co., Ltd.

Address: Building 2, No.388, Binhai 13th Rd., Economic And Technological Development Zone, Wenzhou, Zhejiang, China

Copy of marking plate:



Note:

-Marking plate was silk printed on external enclosure.

-Marking for model K1.22-041(The difference between all model's nameplate is model name)

Photo:

Photo1 External view(K3.0-041)

Photo 2 External view(K3.0-041)

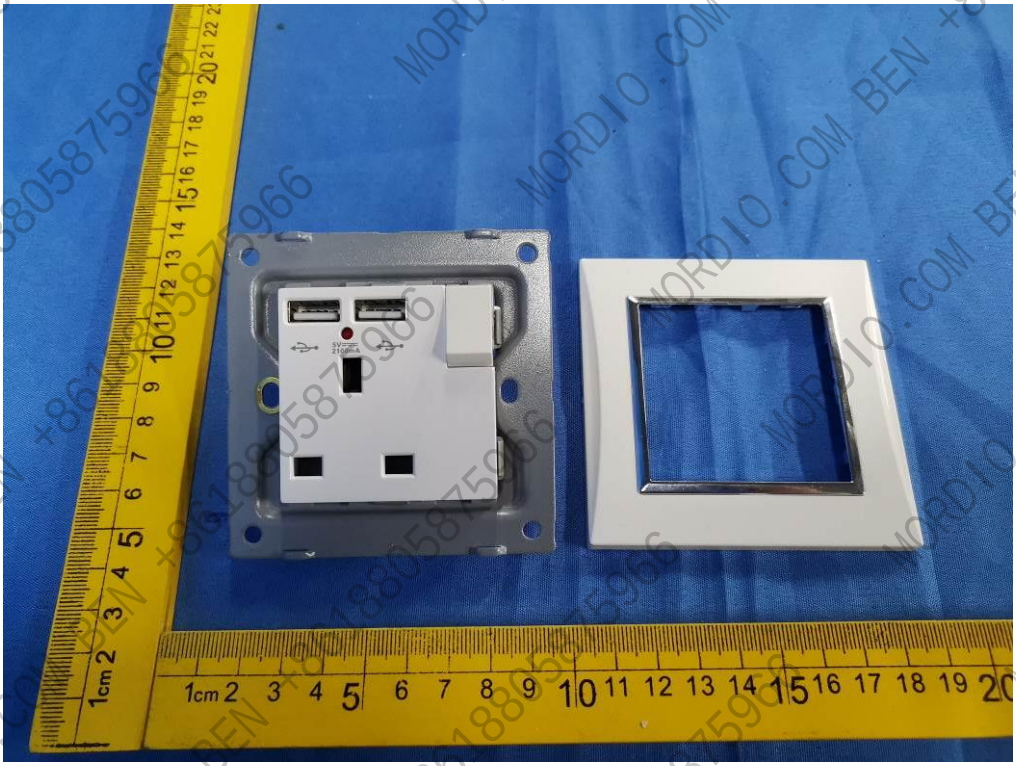


Photo 3 Internal view

Photo 4 Internal view

Photo 5 Internal view

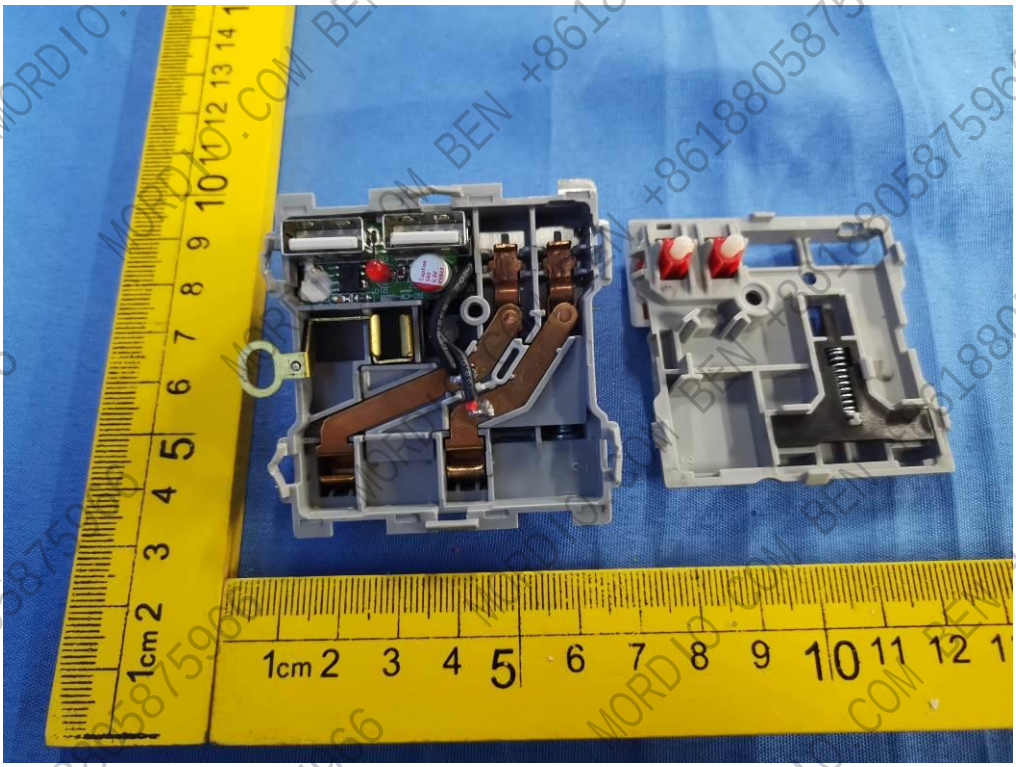


Photo 6 Internal view

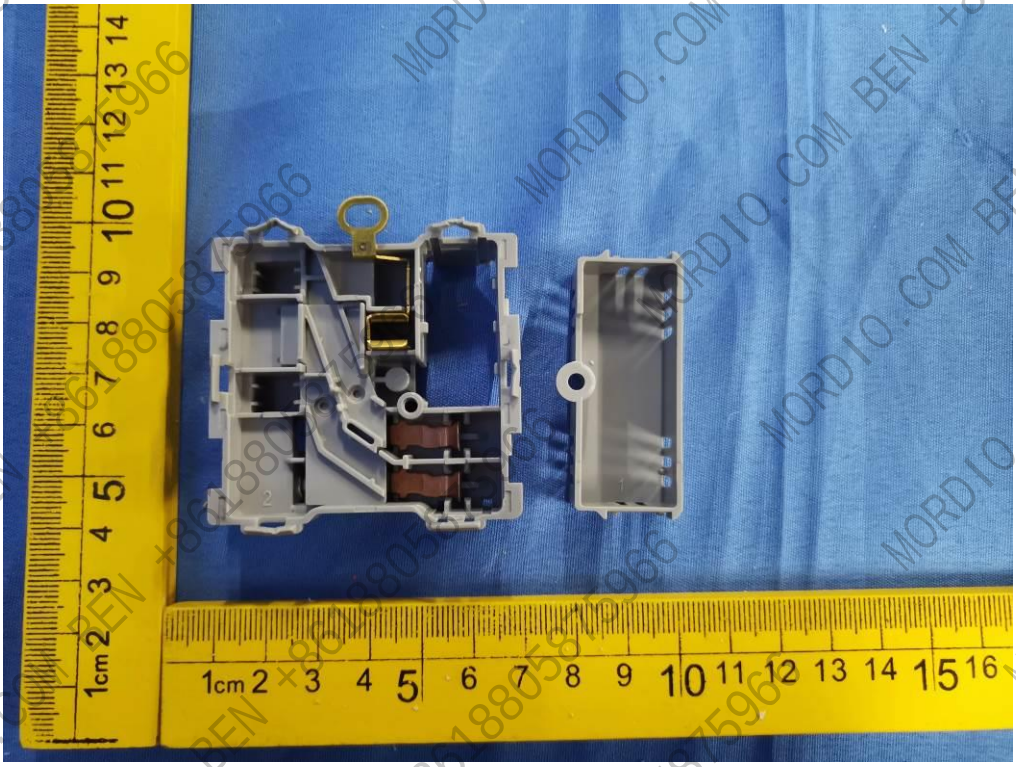


Photo 7 Internal view

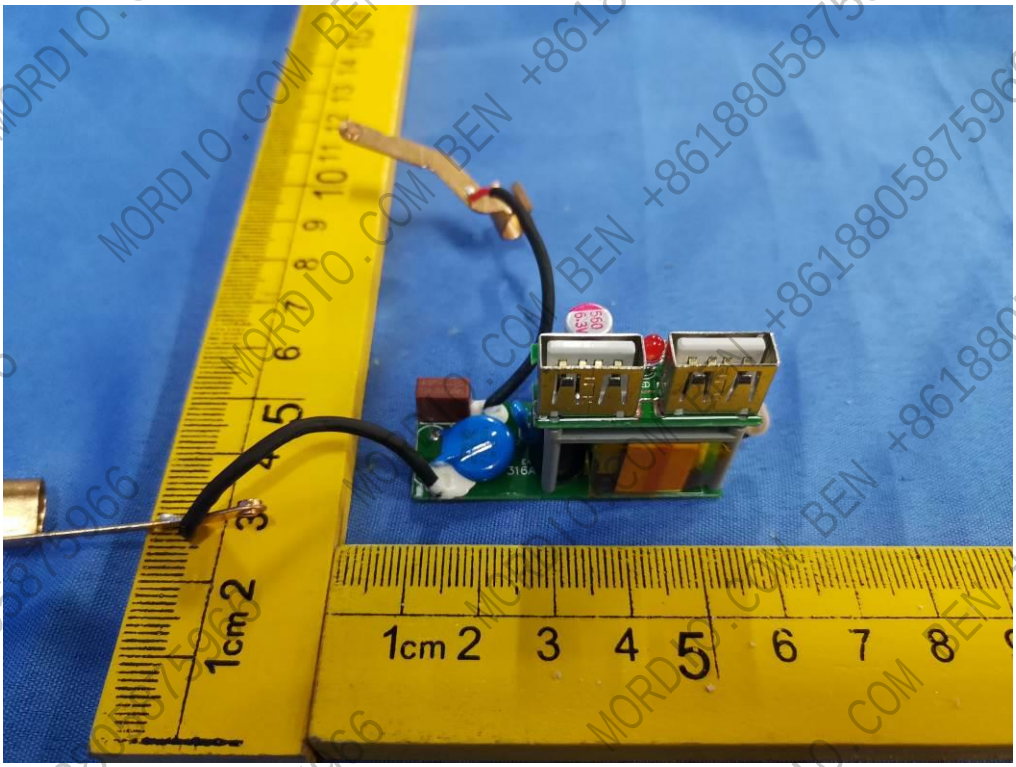


Photo 8 The power supply board

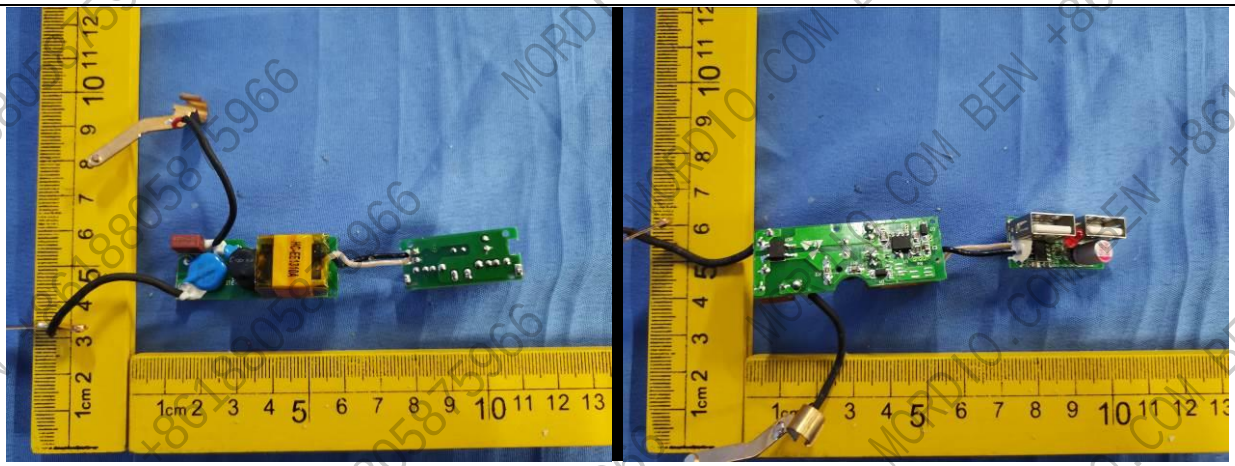


Photo 9 The power supply board

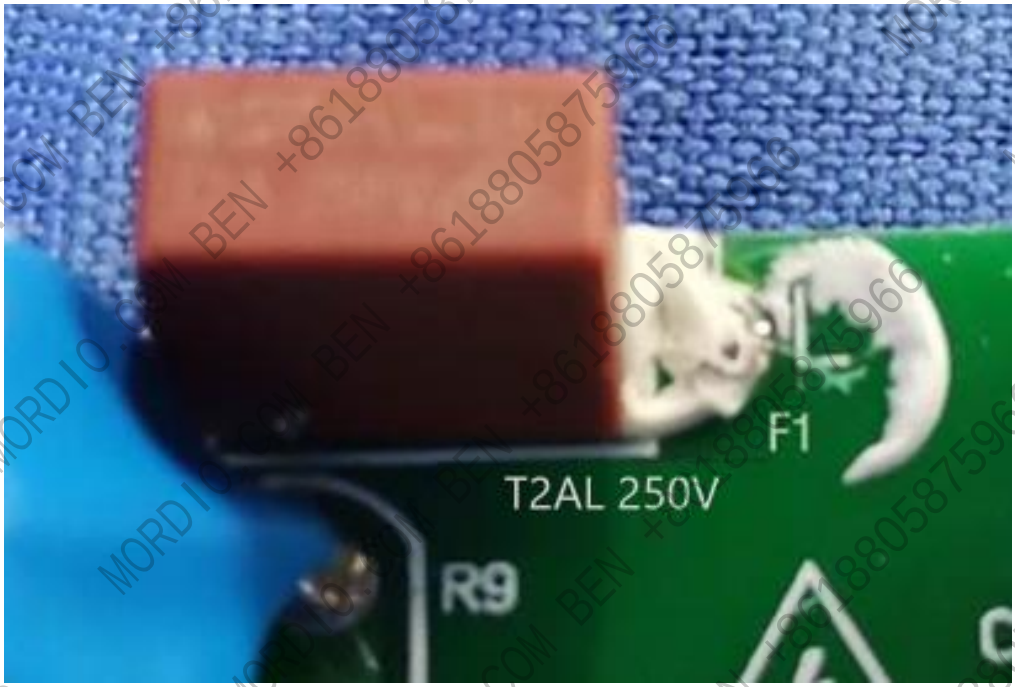


Photo 10 Fuse marking

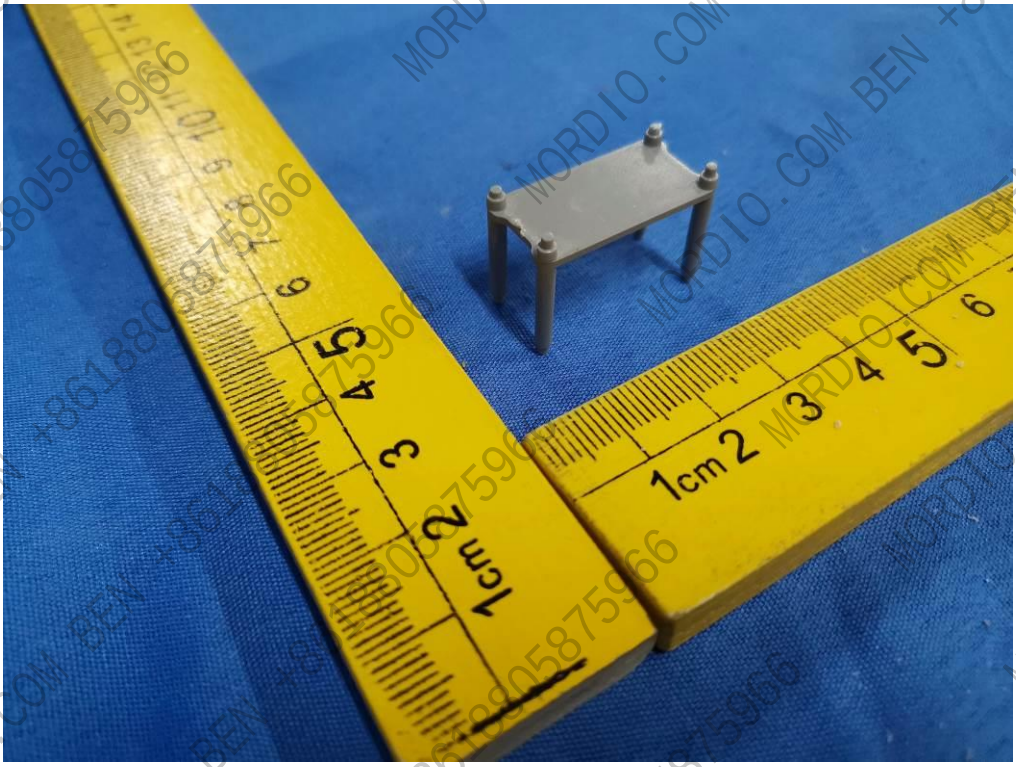


Photo 11 Internal insulation support

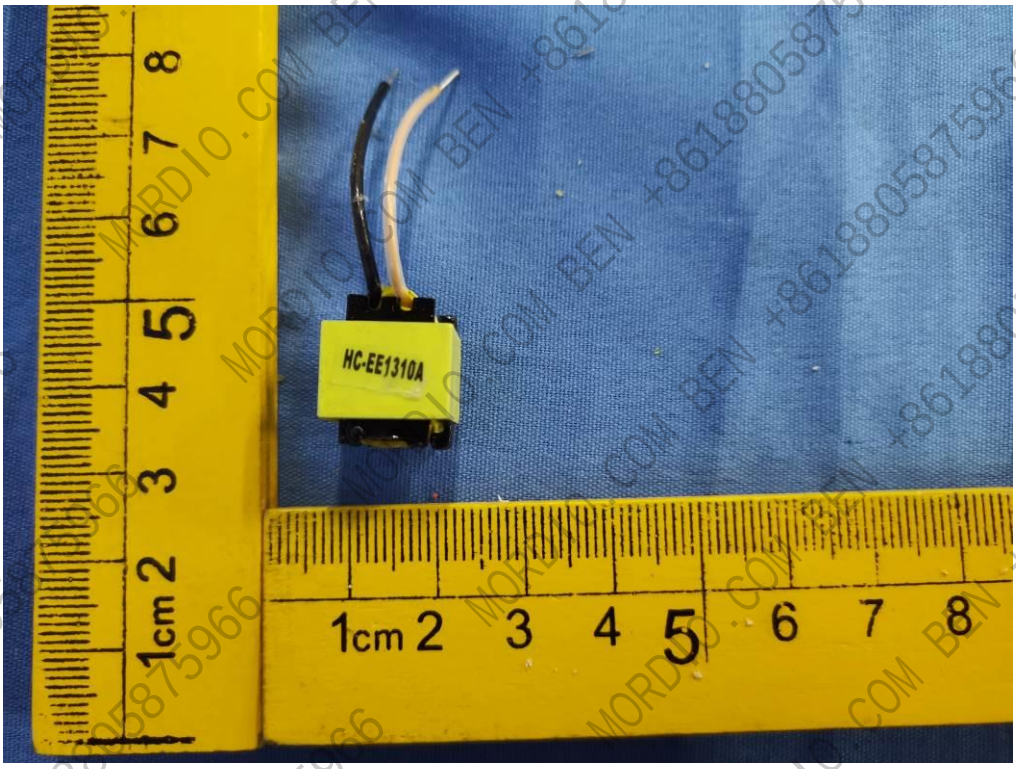


Photo 12 Transformer

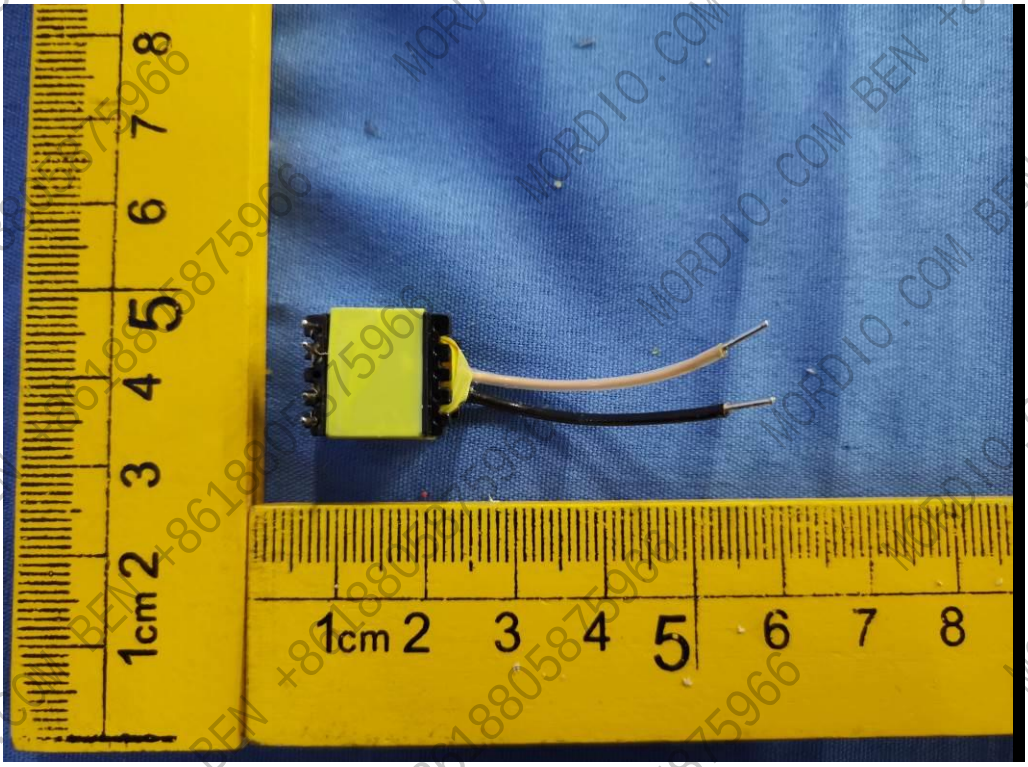


Photo 13 Transformer

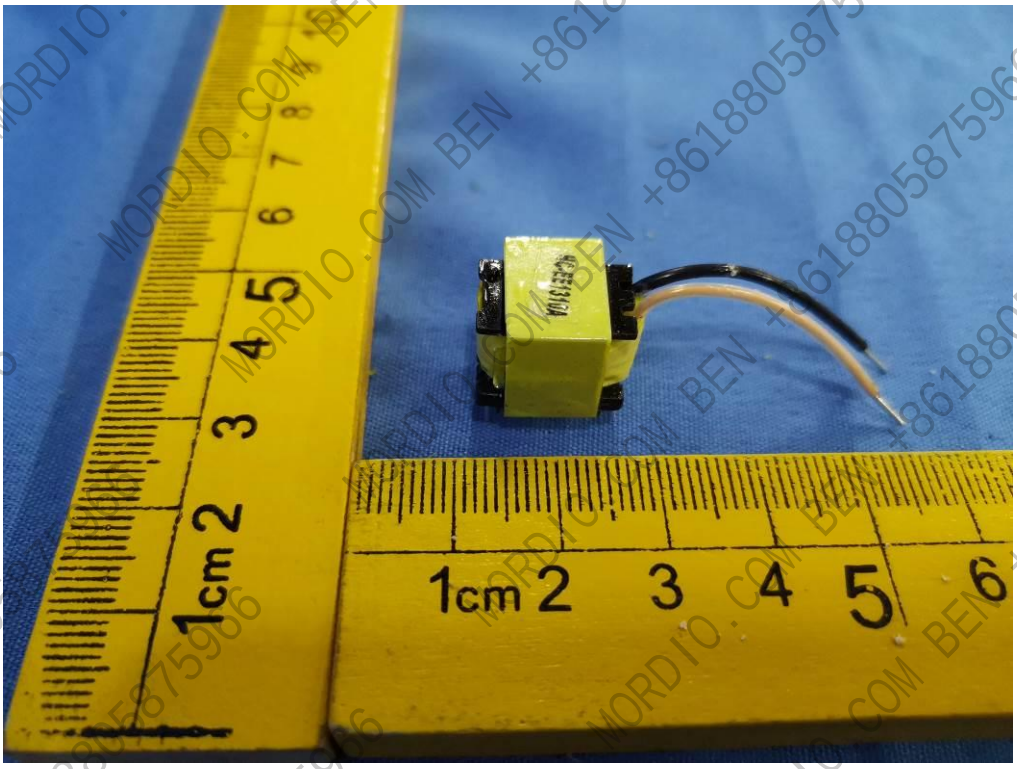


Photo 14 Transformer

Photo 15 External view

Photo 16 External view

Photo 17 External view

Photo 18 External view

Photo 19 External view

Photo 20 External view

Photo 21 External view

Photo 22 External view

Photo 23 External view

Photo 24 External view (S1.1-041)

Photo 25 External view (K1.23-041)

Photo 26 External view (K3.2-041)

Photo 27 External view (K3.2-041)

Photo 28 External view (S1-041)

Photo 29 External view (S1-041)

Photo 30 External view (S1.2-041)

Photo 31 External view (S1.2-041)

Photo 32 External view (S1.3-041)

Photo 33 External view (S1.3-041)

Photo 34 External view (S1.4-041)

Photo 35 External view (S1.4-041)

Photo 36 External view (S5.1-041)

Photo 37 External view (S5.1-041)

Photo 38 External view (S3.1-041)

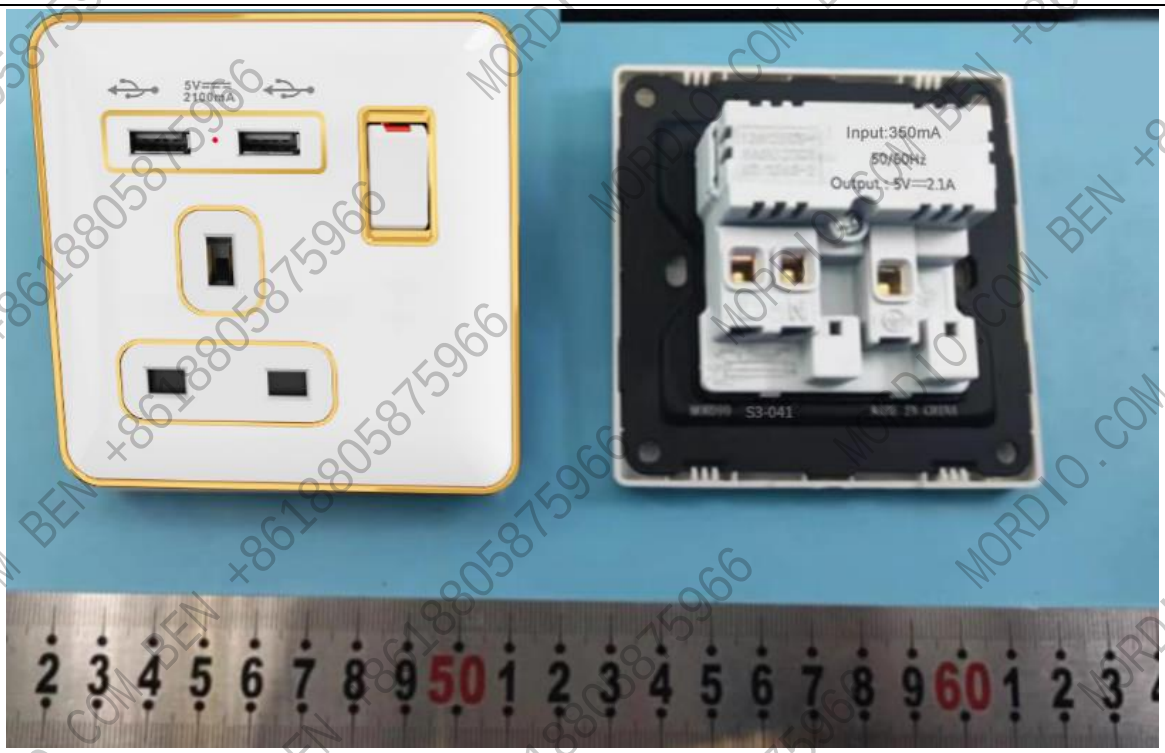


Photo 39 External view (S3-041)

Photo 40 External view (A4-041)

Photo 41 External view (A4-041)

Photo 42 External view (AI-041)

Photo 43 External view (S1.5-041)

Photo 44 External view (L2-041)

Photo 45 External view (L2-041)

Photo 46 External view (S5-041)

Photo 47 External view (S5-041)

Photo 48 External view (T1-041)

Photo 49 External view (T2-041)

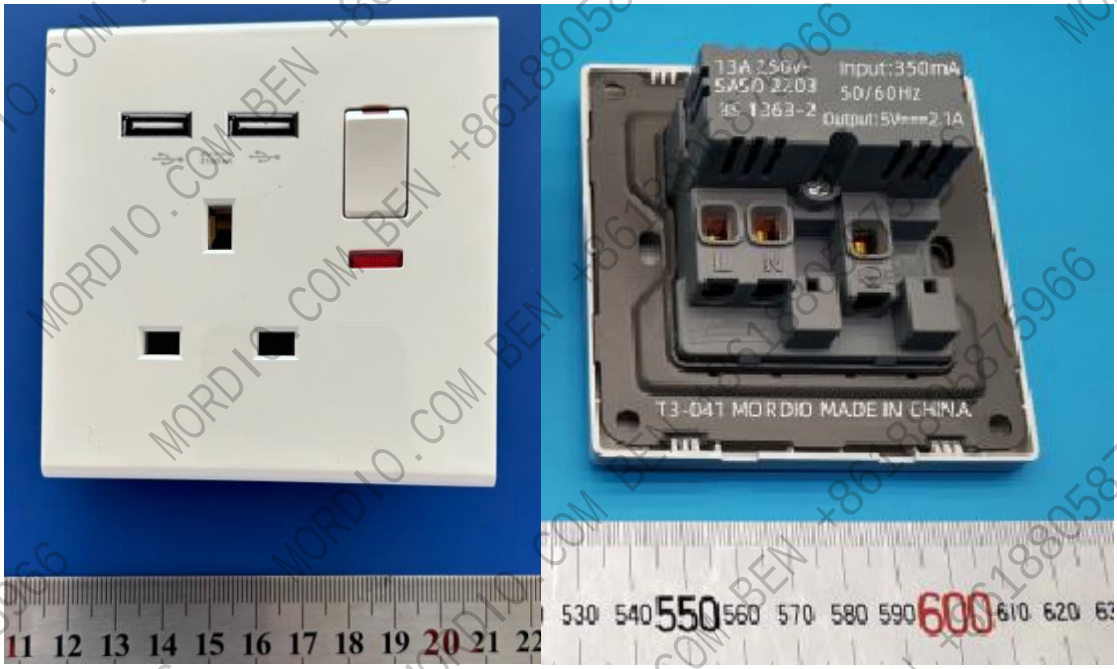


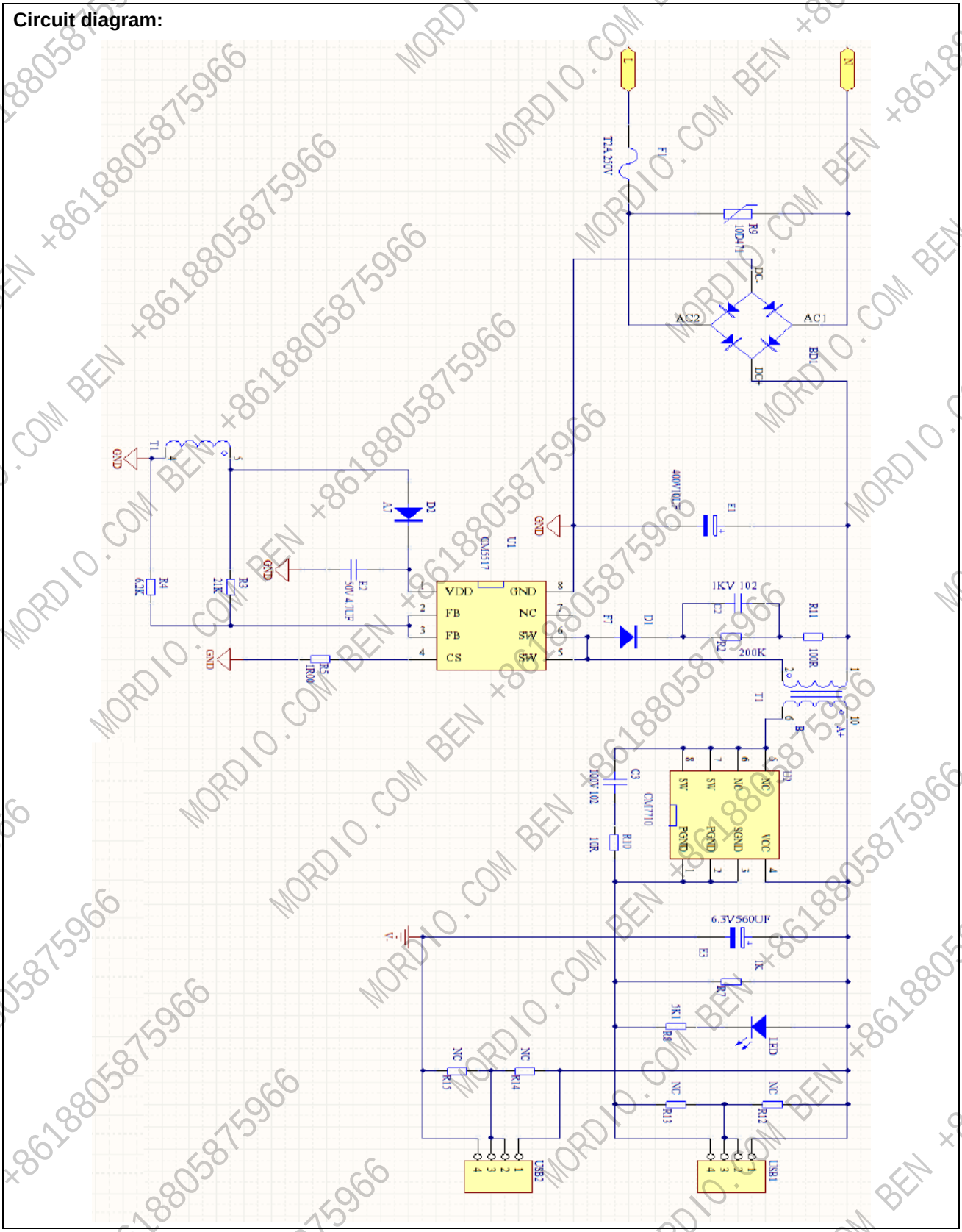
Photo 50 External view (T3-041)

Photo 51 External view (T3.1-041)

Photo 52 External view (T4-041)

Photo 53 External view (T8-041)

Circuit diagram:



BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
3	**Charging Port Detection**		P
3.1	**Overview** Figure 3-1 shows several examples of a PD attached to an SDP or Charging Port.		P
3.2	**Charger Detection Hardware**		P
3.2.1	**Overview** Figure 3-2 shows the charger detection hardware for a PD.		P
3.2.2	**VBUS Detect**		P
	Each PD shall have a session valid comparator that detects when VBUS is greater than its internal session valid threshold. Its internal session valid threshold shall be within VOTG_SESS_VLD.		P
3.2.3	**Data Contact Detect**		N/A
3.2.3.1	**Overview**		N/A
3.2.3.2	**Problem Description**		N/A
3.2.3.3	**Data Contact Detect, Not Attached** Figure 3-4 shows the case where the PD is not attached to a remote device.		N/A
3.2.3.4	**Data Contact Detect, Standard Downstream Port**		N/A
3.2.4	**Primary detection**		P
3.2.4.1	**Primary Detection, DCP** Figure 3-6 shows how Primary Detection works when a PD is attached to a DCP.		P
	During Primary Detection the PD shall turn on VDP_SRC and IDM_SINK. Since a DCP is required to short D+ to D- through a resistance of RDCP_DAT, the PD will detect a voltage on D- that is close to VDP_SRC. A PD shall compare the voltage on D- with VDAT_REF. If D- is greater than VDAT_REF, then the PD is allowed to detect that it is attached to either a DCP or CDP. A PD is optionally allowed to compare D- with VLGC as well, and only determine that it is attached to a DCP or CDP if Dis greater than VDAT_REF, but less than VLGC. The reason for this option is as follows.	Considered	P

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	PS2 ports pull D+/- high. If a PD is attached to a PS2 port, and the PD only checks for Dgreater than V_{DAT_REF}, then a PD attached to a PS2 port would determine that it is attached to a DCP or CDP and proceed to draw I_{DEV_CHG}. This much current could potentially damage a PS2 port. By only determining it is attached to DCP or CDP if D- is less than V_{LGC}, the PD can avoid causing damage to a PS2 port. On the other hand, some proprietary chargers also pull D+/- high. If a PD is attached to one of these chargers, and it determined it was not attached to a charger because D- was greater than V_{LGC}, then the PD would determine that it was attached to an SDP, and only be able to draw I_{SUSP}. The choice of whether or not to compare D- to V_{LGC} depends on whether the PD is more likely to be attached to a PS2 port, or to a proprietary charger.		
3.2.4.2	**Primary Detection, CDP** Figure 3-7 shows how Primary Detection works when a PD is attached to a CDP.		N/A
	A CDP is required to behave in either one of two ways when a remote device is not connected to it. The first way that a CDP is allowed to behave is to enable V_{DM_SRC} within $T_{CP_VDM_EN}$ of a disconnect, and then disable V_{DM_SRC} within $T_{CP_VDM_DIS}$ of a connect. When using this option, a CDP is not required to enable I_{DP_SINK}, or to compare D+ to V_{DAT_REF}. The second way a CDP is allowed to behave is to compare D+ with V_{DAT_REF} and V_{LGC}. When D+ is greater than V_{DAT_REF} and less than V_{LGC}, the CDP shall enable V_{DM_SRC}. When D+ is less than		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	V_{DAT_REF} or greater than V_{LGC}, the CDP shall disable V_{DM_SRC}. Note that a CDP is required to compare D+ to V_{LGC}, in order to disable V_{DM_SRC} when the PD connects. See Section 3.4.2 for timing. During Primary Detection the PD shall turn on V_{DP_SRC} and I_{DM_SINK}. A PD shall compare the voltage on D- with V_{DAT_REF}. If D- is greater than V_{DAT_REF}, then the PD is allowed to determine that it is attached to either a DCP or CDP. A PD is optionally allowed to compare D- with V_{LGC} as well, and only determine that it is attached to a DCP or CDP if D- is greater than V_{DAT_REF}, but less than V_{LGC}. See Section 3.2.4.1 for more details.		
3.2.4.3	**Primary Detection, SDP** Figure 3-8 shows how Primary Detection works when a PD is attached to an SDP.		N/A
	During Primary Detection the PD shall turn on V_{DP_SRC} and I_{DM_SINK}. When a voltage of V_{DP_SRC} is applied to D+, an SDP will continue pulling D- low through R_{DM_DWN}. A PD shall compare the voltage on D- with V_{DAT_REF}. If D- is less than V_{DAT_REF}, then the PD is allowed to determine that it is attached to an SDP. A PD is optionally allowed to compare D- with V_{LGC} as well, and determine that it is attached to an SDP if D- is greater than V_{LGC}. See Section 3.2.4.1 for more details.		N/A
3.2.4.4	**Primary Detection, ACA-Dock** Figure 3-9 shows how Primary Detection works when a PD that supports ACA Detection is attached to an ACA-Dock.		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	An ACA-Dock is a docking station that has one upstream port, and zero or more downstream ports. The upstream port can be attached to a PD, and is capable of sourcing I_{CDP} to the PD. When an ACA-Dock is powered, but nothing is attached to its upstream port, it is required to bias the pins on its upstream port as follows: • VBUS V_{CHG} • D+ V_{DP_UP} • D- V_{DM_SRC} • ID R_{ID_A} • GND GND The VBUS pin is at V_{CHG} because the ACA-Dock is ready to provide power to a PD. The ACA_Dock is required to pull D+ to V_{DP_UP} through R_{DP_UP} because the VBUS pin is greater than $V_{OTG_SESS_VLD}$.		N/A
	An ACA-Dock is required to enable V_{DM_SRC} whenever D+/- have been inactive (at idle J state) for a time of $T_{CP_VDM_EN}$. An ACA-Dock is required to disable V_{DM_SRC} within $T_{CP_VDM_DIS}$ of any activity on D+/-. An ACA-Dock is required to present an impedance to ground on ID of R_{ID_A} whenever it is powered. It is required to present an impedance to ground on ID of R_{ID_FLOAT} when it is not powered. When a PD that supports ACA detects the following conditions, it shall determine that it is attached to an ACA-Dock: • VBUS > $V_{OTG_SESS_VLD}$ • D+ at V_{LGC_HI} • V_{DAT_REF} < D- < V_{LGC} • ID at R_{ID_A} Note that a PD attached to an ACA-Dock is required to compare D- with V_{LGC}. If a PD were attached to an ACA that had a LS peripheral on its Accessory Port, then the ID pin of the PD would be pulled to ground through R_{ID_A}, and the D- pin would be at V_{LGC_HI} instead of V_{DM_SRC}. In order to distinguish between an ACA with a LS device and an ACA-Dock, the PD is required to detect if D- is above or below V_{LGC}. The V_{DP_SRC} in the PD shall be such that D+ remains at a logic high while the ACA-Dock is pulling D+ to V_{DP_UP} through R_{DP_UP}. The reason for this is so that the ACA-Dock does not detect activity on D+, which could cause it to turn off its V_{DM_SRC} before the PD completes its Primary Detection.		N/A
3.2.4.5	**Primary Detection, Micro ACA** Figure 3-10 shows how Primary Detection works when a PD that supports ACA Detection is attached to a Micro ACA.		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	A PD that supports ACA Detection is required to monitor the resistance on the ID pin whenever VBUS is greater than $V_{OTG_SESS_VLD}$. If the ID resistance is R_{ID_B} or R_{ID_C}, then the PD knows that it is attached to an ACA. If the ID resistance is R_{ID_A}, then the PD could be attached to either an ACA with a B-device on its Accessory Port, or to an ACA-Dock. In order to distinguish between an ACA with an B-device, and an ACA-Dock, the PD shall compare the voltage on D- with V_{DAT_REF} and V_{LGC} to detect what it is attached to as follows: • D- < V_{DAT_REF} ACA with FS B-device on Accessory Port • V_{DAT_REF} < D- < V_{LGC} ACA-Dock • V_{LGC} < D- ACA with LS B-device on Accessory Port The PD shall do the above detection on D- after attach, and before connect, as shown in the Good Battery Algorithm. After doing Primary Detection, a PD that supports ACA Detection shall continue to monitor the ID line. If this resistance changes, the PD shall respond according to the state machine defined in Section 6.2.7. An ACA is required to do a form of Primary Detection over the DP_CHG and DN_CHG lines to detect if a Charging Port is attached to the ACA Charger Port. This detection is done with the lines highlighted in yellow, and is described in Section 6.2.6.		N/A
3.2.5	**Secondary Detection**		N/A
	Secondary Detection can be used to distinguish between a DCP and a CDP. PDs that are not ready to be enumerated within $T_{SVLD_CON_PWD}$ of detecting VBUS are required to implement Secondary Detection. PDs that are ready to be enumerated are allowed to bypass Secondary Detection. See Section 3.3.2 on Good Battery Algorithm.		N/A
3.2.5.1	**Secondary Detection, DCP** Figure 3-11 shows how Secondary Detection works when a PD is attached to a DCP.		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	During Secondary Detection, a PD shall output V_{DM_SRC} on D-, turn on I_{DP_SINK}, and compare the voltage on D+ to V_{DAT_REF}. Since a DCP is required to short D+ to D- through a resistance of R_{DCP_DAT}, the voltage on D+ will be close to V_{DM_SRC}, which is above V_{DAT_REF}. If a PD detects that D+ is greater than V_{DAT_REF}, it knows that it is attached to a DCP. It is then required to enable V_{DP_SRC} or pull D+ to V_{DP_UP} through R_{DP_UP}, as defined in the Good Battery Algorithm in Section 3.3.2. A PD is not required to compare D+ to V_{LGC} during Secondary Detection.		N/A
3.2.5.2	**Secondary Detection, CDP** Figure 3-12 shows how Secondary Detection works when a PD is attached to a CDP.		N/A
	During Secondary Detection, a PD shall output V_{DM_SRC} on D-, turn on I_{DP_SINK}, and compare the voltage on D+ to V_{DAT_REF}. Since a CDP does not short D+ to D-, the voltage on D+ will be close to ground, which is below V_{DAT_REF}. If a PD detects that D+ is less than V_{DAT_REF}, it knows that it is attached to a CDP. It is then required to turn off V_{DP_SRC} and V_{DM_SRC}, as shown in the Good Battery Algorithm in Section 3.3.2, and is allowed to draw I_{DEV_CHG}. A PD is not required to compare D+ to V_{LGC} during Secondary Detection.		N/A
3.2.6	**ACA Detection**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	ACA Detection allows a PD to detect when it is attached to an ACA, and to detect what type of device is attached to the ACA Accessory Port. See Section 6 for a description of the ACA. A PD is not required to support ACA Detection. Only PDs that have a Micro-AB receptacle can support ACA Detection, since the ACA OTG Port has a captive cable terminating in a Micro-A plug. PDs that support ACA Detection are required to implement the Good Battery Algorithm defined in Section 3.3.2. Figure 3-13 shows how ACA Detection works when a PD is attached to a Micro ACA. A PD detects the presence of an ACA by sensing the resistance on the ID pin. There are five different resistance values that shall be detected during ACA Detection, namely: R_{ID_GND}, R_{ID_C}, R_{ID_B}, R_{ID_A} and R_{ID_FLOAT}. PDs that support ACA Detection shall monitor the ID resistance during the entire time that VBUS is asserted, and respond according to the PD State Machine in Section 6.2.7.		N/A
3.3	**Charger Detection Algorithms**		N/A
3.3.1	**Weak Battery Algorithm** Figure 3-14 shows an example charger detection algorithm for a PD with a Weak Battery. Other algorithms are allowed, providing they comply with the DBP.		N/A
	A PD is required to have internal voltage thresholds that lie within $V_{OTG_SESS_VLD}$, V_{DAT_REF} and V_{LGC}. In the above algorithm, a PD compares VBUS, D+ and D- with its internal thresholds. It does not compare VBUS, D+ and D- with the min or max value of $V_{OTG_SESS_VLD}$, V_{DAT_REF} or V_{LGC}. In the above example, a PD with a Weak Battery detects VBUS greater than $V_{OTG_SESS_VLD}$, and applies a voltage of V_{DP_SRC} on the D+ pin. If the voltage on D- is greater than its V_{DAT_REF}, or if the ID pin is not floating, the PD is allowed to draw I_{DEV_CHG}. Else the PD is allowed to draw I_{UNIT}. The V_{LGC} term shown in magenta could be added to prevent a PD from charging from PS2 ports and some proprietary chargers.		N/A
3.3.2	**Good Battery Algorithm**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	Figure 3-15 shows the charger detection algorithm that a PD with a Good Battery is required to implement. It may also be used by a PD with a Weak Battery, subject to meeting the requirements of the Dead Battery Provision. Thus a PD, having reached the bottom of the flow chart may in all cases, with the exception of the DCP/CDP exit, delay for up to $T_{SVLD_CON_WKB}$ before connecting or applying a bus reset as appropriate. A PD shall implement the Good Battery Algorithm when attached to an SDP or Charging Port. A PD is allowed to include additional branches for detecting devices or ports other than an SDP or Charging Port. Any such branches shall not cause additional activity on D+/- and/or ID that would interfere or be confused with the next expected event when the PD is attached to an SDP or Charging Port. Branches are also allowed after any final step in detection, and these branches may include additional activity on D+/- and/or ID, except that when a PD is attached to a DCP, it shall maintain D+ greater than V_{DAT_REF} while VBUS is asserted. Upon detecting VBUS greater than its $V_{OTG_SESS_VLD}$ threshold, a PD shall start a timer with a timeout value of $T_{DCD_TIMEOUT}$. A PD that supports DCD is allowed to enable its I_{DP_SRC} and monitor for D+ being at V_{LGC_LOW} for T_{DCD_DBNC}. A PD that supports ACA Detection is allowed to monitor for ID not floating for T_{DCD_DBNC}. If the DCD timer expires before the D+ or ID conditions are detected, the PD shall proceed to Primary Detection. If a PD detects that ID is not floating for a time of T_{DCD_DBNC}, then it is allowed to proceed directly to one of the ACA states, without having to do Primary Detection and without having to assert V_{DP_SRC}.		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	During Primary Detection, a PD shall enable V_{DP_SRC}, and compare D- with V_{DAT_REF}. A PD may optionally compare D- with V_{LGC} to avoid damaging a PS2 port. See Section 3.2.4.1. A PD that supports ACA Detection is required to detect the resistance on the ID line. If a PD Detects that it is attached to either a DCP or CDP during Primary Detection, and it is ready to be enumerated, then it is allowed to take the branch where it connects. If a PD is not ready to be enumerated, then it is required to do Secondary Detection. During Secondary Detection, the PD shall disable V_{DP_SRC}, enable V_{DM_SRC} and compare D+ with V_{DAT_REF}. If D+ is greater than V_{DAT_REF}, then the PD is attached to a DCP. The PD shall disable V_{DM_SRC}, and either enable V_{DP_SRC} or pull D+ to V_{DP_UP} through R_{DP_UP}. If D+ is less than V_{DAT_REF}, then the PD is attached to a CDP. The PD shall disable V_{DM_SRC}, and leave both D+ and D- low until it is ready to connect and be enumerated. A PD that is attached to a DCP shall either enable V_{DP_SRC} or pull D+ high within $T_{SVLD_CON_PWD}$ of attach. A PD that supports ACA Detection is required to monitor the resistance on the ID line. If a resistance of R_{ID_A} is detected, then the PD shall compare D- with both V_{DAT_REF} and V_{LGC}, to determine if it is attached to an ACA-Dock or an ACA-A. See Section 3.2.4.4 for more details.		N/A
3.4	**Charger Detection Timing**		P
3.4.1	**Data Contact Detect Timing**		P
	To initiate Data Contact Detect, the PD shall enable I_{DP_SRC} and either I_{DM_SINK} or R_{DM_DWN}. When the PD detects that the D+ line has been low for a time of T_{DCD_DBNC}, then the PD knows that the data pins have made contact Figure 3-16 shows the timing associated with Data Contact Detect (DCD) when pins make contact after DCD starts. Figure 3-17 shows the timing associated with Data Contact Detect when pins have made contact before DCD starts.		P
3.4.2	**Detection Timing, CDP**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	Figure 3-19 shows the timing associated with Primary and Secondary Detection when a PD is attached to a CDP, for the case where the CDP compares D+ to V_{DAT_REF} and V_{LGC}, and enables V_{DM_SRC} accordingly. A CDP is also allowed to leave V_{DM_SRC} enabled while a remote device is not connected. See Section 3.2.4.2 for more details. Figure 3-19 shows the Primary and Secondary Detection timing for a PD attached to a CDP. During Primary Detection, the PD turns on V_{DP_SRC} and I_{DM_SINK}. The CDP is required to have V_{DM_SRC} on D- within a time of T_{VDMSRC_EN} from when D+ is above V_{DAT_REF}. After a time of T_{VDPSRC_ON}, the PD is allowed to check the status of the D- line. If D- is above V_{DAT_REF} (and optionally below V_{LGC}, see Section 3.2.4.1) then the PD is attached to a Charging Port, and is allowed to draw I_{DEV_CHG}. In order to do Secondary Detection, the PD is required to disable V_{DP_SRC} and I_{DM_SNK}, and enable V_{DM_SRC} and I_{DP_SINK}. After a time of T_{VDMSRC_ON}, the PD is allowed to check the status of the D+ line. Since a CDP does not source a voltage on D+, D+ is below V_{DAT_REF} and the PD is attached to a CDP. If the PD was powered up at the time VBUS was detected, then it shall connect within a time of $T_{SVLD_CON_PWD}$. The CDP shall disable I_{DP_SINK} within $T_{CON_IDPSNK_DIS}$ of detecting the connect.		N/A
3.5	**Ground Current and Noise Margins**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	As shown in Figure 7-47 of the USB 2.0 specification, a current of 100 mA through the ground wire of a USB cable can result in a voltage difference of 25 mV between the host ground and the device ground. This ground difference has the effect of reducing noise margins for both signaling and charger detection. The maximum current that a PD is allowed to draw from a CDP is I_{DEV_CHG}. A PD that draws more than I_{CFG_MAX} from a CDP is required to support LS, FS, HS and chirp signaling when the local ground is V_{GND_OFFSET} max higher than the remote ground. A host port that grants the CDP handshake is required to support LS, FS, HS and chirp signaling when the local ground is V_{GND_OFFSET} max lower than the remote ground. When the ground offset is V_{GND_OFFSET} max, the PD and CDP are required to have a greater common mode range than what is called out in USB 2.0.		N/A
4	**Charging Port and Portable Device Requirements**		P
	This section describes the requirements for the following: • Charging Downstream Port (CDP) • ACA-Dock • Dedicated Charging Port (DCP) • Accessory Charger Adapter (ACA) • Portable Device (PD)	DCP considered	P
4.1	**Charging Port Requirements**		P
	The following requirements apply to all types of Charging Ports, including CDP, ACA-Dock, DCP and ACA.	DCP considered	P
4.1.1	**Overshoot**		P
	The output voltage of a Charging Port shall not exceed V_{CHG_OVRSHT} for any step change in load current, nor when the Charging Port is powered on or off.	Not exceed 6.0V	P
4.1.2	**Maximum Current**		P
	The output current of a Charging Port shall not exceed I_{CDP} max under any condition.	Maximum output current of submitted sample is max.2.1A.	P
4.1.3	**Detection Renegotiation**		P

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Clause	Requirement + Test	Result - Remark	Verdict
	A downstream port is allowed to act as an SDP, CDP or DCP, and to change between these roles. In order to force an attached PD to repeat the charging detection procedure, a downstream port is required to: • stop driving VBUS • allow VBUS to drop to less than V_{BUS_LKG} • wait for a time of T_{VBUS_REAPP} • start driving VBUS	Considered.	P
4.1.4	**Shutdown Operation**		P
	If the current drawn by a PD causes a Charging Port to go outside of its Required Operating Range, then the Charging Port is allowed to shut down. All types of shut down are allowed outside the Required Operating Range of a Charging Port, including: • Turning off VBUS • Constant current limiting • Foldback current limiting	Considered	P
4.1.5	**Failure Voltage**		P
	The output voltage of a Charging Port shall remain within V_{CHG_FAIL} for any single point failure in the Charging Port.	Considered	P
4.1.6	**Multiple Ports**		N/A
	For a device with multiple Charging Ports, each Charging Port shall stay within its Required Operating Range regardless of the operation of the other Charging Ports.		N/A
4.2	**Charging Downstream Port** The following requirements apply to a CDP.		N/A
4.2.1	**Required Operating Range**		N/A
	A CDP shall output a voltage of V_{CHG} for all currents less than I_{CDP} min. The voltage on VBUS is averaged over a time of T_{VBUS_AVG}. For load currents greater than I_{CDP} min, a CDP is allowed to shut down. Once in shutdown, the requirements in Section 4.1.4 apply. Figure 4-1 shows several example load curves for a CDP. Load curves are required to cross the line at I_{CDP} min within a voltage range of V_{CHG}. Load curves that cross the line at V_{CHG} min for currents less than I_{CDP} min are not allowed.		N/A
4.2.2	**Shutdown Operation**		N/A
	If a CDP goes into shutdown during a current overload condition, it shall recover and output a voltage of V_{CHG} within a time of T_{SHTDWN_REC} when the current overload condition has been removed.		N/A
4.2.3	**Undershoot**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	The output voltage of a CDP shall be within V_{CHG_UNDSHT} for any step change in load currents that are less than I_{CDP} min.		N/A
4.2.4	**Detection Signaling**		N/A
	A CDP is required to behave in either one of two ways when a remote device is not connected to it. The first way that a CDP is allowed to behave is to enable V_{DM_SRC} within $T_{CP_VDM_EN}$ of a disconnect, and then disable V_{DM_SRC} within $T_{CP_VDM_DIS}$ of a connect. When using this option, a CDP is not required to enable I_{DP_SINK}, or to compare D+ to V_{DAT_REF}. The second way a CDP is allowed to behave is to compare D+ with V_{DAT_REF} and V_{LGC}. When D+ is greater than V_{DAT_REF} and less than V_{LGC}, the CDP shall enable V_{DM_SRC}. When D+ is less than V_{DAT_REF} or greater than V_{LGC}, the CDP shall disable V_{DM_SRC}. See Section 3.4.2 for timing.		N/A
4.2.5	**Connector**		N/A
	A CDP shall have a Standard-A receptacle.		N/A
4.3	**ACA-Dock**		N/A
	The following requirements apply to the upstream port of an ACA-Dock.		N/A
4.3.1	**Required Operating Range**		N/A
	An ACA-Dock shall have the same Required Operating Range as a CDP.		N/A
4.3.2	**Undershoot**		N/A
	An ACA-Dock shall comply with the same undershoot requirements as a CDP.		N/A
4.3.3	**Detection Signaling**		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	When a PD is attached to an ACA-Dock, the PD acts as host while drawing current from VBUS. This is similar to the case where a PD is attached to an ACA with a peripheral on the Accessory Port. To inform the PD that it should act as host and draw current, both the ACA-Dock and the ACA are required to pull the ID pin to ground through a resistance of R_{ID_A}. An ACA-Dock is required to provide I_{CDP} to the PD, whereas an ACA is required to provide I_{DCP}, and this must be shared between the PD and whatever is on the Accessory Port. To inform the PD that it is attached to an ACA-Dock as opposed to an ACA, the ACA-Dock shall output a voltage of V_{DM_SRC} on D- as follows: • ACA-Dock shall start outputting V_{DM_SRC} if D+/- are at idle J for a time of $T_{CP_VDM_EN}$ • ACA-Dock shall stop outputting V_{DM_SRC} within $T_{CP_VDM_DIS}$ of any USB activity on D+/-		N/A
4.3.4	**Connector**		N/A
	An ACA-Dock shall have a Micro-A plug that can be mated to the Micro-AB receptacle of a PD.		N/A
4.4	**Dedicated Charging Port**		P
	The following requirements apply to a DCP.		P
4.4.1	**Required Operating Range**		P
	A DCP shall output a voltage of V_{CHG} for all currents less than I_{DCP} min. The voltage on VBUS is averaged over a time of T_{VBUS_AVG}. A DCP shall not shut down if the load current is less than I_{DEV_CHG} and the load voltage is greater than $V_{DCP_SHTDOWN}$. A DCP is allowed to shut down for load currents greater than I_{DEV_CHG} max, or for load voltages less than V_{DCP_SHTDWN}. Once in shutdown, the requirements in Section 4.1.4 apply. Figure 4-2 shows several example load curves. DCP load curves are required to cross the constant current line at I_{DEV_CHG} max, or the constant voltage line at V_{DCP_SHTDWN}. A DCP is not allowed to shut down in the Required Operating Range.	5.162Vdc	P
4.4.2	**Undershoot**		P

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Clause	Requirement + Test	Result - Remark	Verdict
	For step changes in load current from I_{DCP_LOW} to I_{DCP_MID}, or from I_{DCP_MID} to I_{DCP_HI}, the undershoot voltage of a DCP shall be V_{CHG_UNDSHT}. DCPs are required to meet this requirement for load steps from mid to hi that occur $T_{DCP_LD_STP}$ after the transition from low to mid. The duration of the undershoot shall be T_{DCP_UNDSHT}.	Min. 5.035V dc (for step changes in load current from IDCP_LOW to IDCP_MID) Min. 4.760V dc (for step changes in load current from IDCP_MID to IDCP_HI)	P
	For step changes in load current from I_{DCP_LOW} to I_{DCP_HI}, the output voltage of a DCP is allowed to drop to the load voltage of the attached PD for a time of T_{DCP_UNDSHT}. After this time, the output voltage of a DCP shall be at V_{CHG} for load currents less than I_{DCP} min.	The output voltage is in range of 4.75 – 5.25Vdc.	P
4.4.3	**Detection Signaling**		P
	A DCP shall have an impedance between D+ and D- of R_{DCP_DAT}.	Less than 200Ω between D+ and D-	P
	The leakage current on the D+/- pins of a DCP shall be less than or equal to the leakage current that would occur from two resistances of R_{DAT_LKG} tied to a voltage of V_{DAT_LKG}. See Figure 3-6.	Excessive Leakage sourced by D+/D- in spec (U = 0.005 V)	P
	The capacitance between the D+/- pins and ground of a DCP shall be C_{DCP_PWR}.	Capacitance is less than 1nF	P
4.4.4	**Connector**		P
	A DCP shall have a Standard-A receptacle, or a captive cable terminated with a Micro-B plug.	With a standard-A receptacle	P
4.5	**Accessory Charger Adapter**		N/A
	The following requirements apply to an ACA with a DCP or CDP on its Charger Port.		N/A
4.5.1	**Required Operating Range**		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	The Required Operating Range for the OTG Port of an ACA is affected by the following factors: • Device on Charger Port (DCP or CDP) • Current drawn from Accessory Port • RACA_CHG_OTG • VACA_OPR The current available on the OTG Port is determined by how much current is supplied to the Charger Port, and how much current is being drawn from the Accessory Port. The voltage available on the OTG Port is determined by the voltage at the Charger Port, the current being drawn from the OTG and Accessory Ports, and RACA_CHG_OTG. ACA operation is only required if for Charger Port voltages in the range of VACA_OPR.		N/A
4.5.2	**Undershoot**		N/A
	An ACA with a DCP or CDP on its Charger Port shall comply with the same undershoot requirements as a DCP.		N/A
4.5.3	**Detection Signaling**		N/A
	An ACA shall pull the ID pin of the OTG port to ground through one of the following resistances, as specified in Section 6: • RID_GND, RID_C, RID_B, RID_A, RID_FLOAT An ACA shall connect the data pins of the OTG Port directly to the data pins of the Accessory Port.		N/A
4.5.4	**Connector**		N/A
	An ACA shall have a captive cable terminated with a Micro-A plug on its OTG Port.		N/A
4.6	**Portable Device** The following requirements apply to a PD.		N/A
4.6.1	**Allowed Operating Range**		N/A
	A PD shall not draw more than IDEV_CHG max from a Charging Port. A PD shall not pull the output voltage of a Charging Port below VDCP_SHTDWN max. Figure 4-3 shows the Allowed Operating Range for a PD.		N/A
4.6.2	**Detection Signaling**		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	All PDs shall implement the following detection features: • DCD timer (TDCD_TIMEOUT) • Primary Detection – To detect between DCP, CDP and SDP – Compare D- to VDAT_REF during Primary Detection PDs are allowed, but not required, to implement the following detection features: • DCD, using IDP_SRC • Compare D- to VLGC during Primary Detection • Secondary Detection • ACA Detection		N/A
4.6.3	**Detection Renegotiation**		N/A
	To restart the charger detection procedure, a downstream port is allowed to remove and then re-assert power on VBUS. See Section 4.1.3. In order to detect this drop in VBUS, a PD shall discharge VBUS to less than VBUS_LKG within TVLD_VLKG whenever VBUS is removed. A PD is allowed to disconnect and repeat the charger detection process multiple times while attached. The PD is required to wait for a time of at least TCP_VDM_EN max between disconnecting and restarting the charger detection process.		N/A
4.6.4	**Connector**		N/A
	A PD that mates with an ACA-Dock or ACA shall have a Micro-AB receptacle.		N/A

5	**Parameter Values**		--

6.1	**Charger Port on ACA**		N/A
	ACA shall indicate when Charger Port can provide power to other ports.		N/A
	If not a combined charger, an ACA is required to label the Charger Port as Charger Only		N/A
	An ACA has the following three ports: OTG Port Accessory Port Charger Port		N/A
	OTG Port shall have a captive cable that terminates with a Micro-A plug, only OTG devices can be attached to the OTG Port.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Accessories attached to the Accessory Port can communicate with the OTG device using normal USB signaling.		N/A
	Type of ACA: - Micro ACA or Standard ACA		N/A
6.2.1	Micro ACA Ports		N/A
	Cables can be uses to attach the Accessory Port of a Micro ACA to an accessory		N/A
	A Micro ACA Charger Port connector		N/A
6.2.6	Micro ACA Requirements		N/A
	A Micro ACA Charger Port shall draw less than ISUSP when anything other than a Charging Port is attached to it.		N/A
	A Micro ACA shall draw less than ISUSP when a Charging Port is attached to the ACA Charger Port and nothing is attached to the OTG Port or Accessory Port.		N/A
	The resistance between the VBUS_CHG and VBUS_OTG pins of an ACA shall be RACA_CHG_OTG when the Charger Switch is closed in rows 5-8 of Table 6-2, and the voltage on VBUS_CHG is at VACA_OPR.		N/A
	The resistance between the VBUS_CHG and VBUS_ACC pins of an ACA shall be RACA_CHG_ACC when both the Charger Switch and the Accessory Switch are closed in row 6 of Table 6-2, and the voltage on VBUS_CHG is at VACA_OPR.		N/A
	The resistance between the VBUS_OTG and VBUS_ACC pins of an ACA shall be RACA_OTG_ACC when the Charger Switch is open and the Accessory Switch is closed in rows 2b and 4 of Table 6-2 and the voltage on either VBUS_ACC or VBUS_OTG is at VACA_OPR.		N/A
	The resistance between the VBUS_OTG and VBUS_ACC pins of an ACA shall be RADP_OTG_ACC when the Accessory Switch is in condition ADP-pass in rows 1, 2a or 3 of Table 6-2.		N/A
	The resistance between the internal ground of the Micro ACA and the ground pin of a Micro- AB receptacle attached to the OTG port of an ACA shall be ROTG_ACA_GND. This requirement limits the difference between OTG and ACA ground under conditions of high charging current. This in turn allows the OTG device to reliably detect the ACA ID resistance under conditions of high charging current.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	When a Micro ACA detects VBUS_CHG asserted, it shall output VDP_SRC on DP_CHG. If the ACA detects DN_CHG greater than VDAT_REF, then it is allowed to close its Charger Switch for as long as VBUS_CHG remains above VOTG_SESS_VLD. Note that this could result in the ACA drawing more than ICFG_MAX from a PS2 port.		N/A
	If the Charger Port was attached to a CDP, then it's possible that DN_CHG may go below VDAT_REF of the ACA due to charging currents causing the CDP ground to be lower than the ACA ground. It's also possible that the CDP could issue a USB reset. The ACA shall ignore either of these effects, and continue to leave its Charger Switch closed. When VBUS_CHG goes below VOTG_SESS_VLD, then the ACA is required to again check for VDN_CHG being greater than VDAT_REF, before opening the Charger Switch.		N/A
	The Micro ACA is required to have a capacitance of CMACA_VBUS on both the VBUS_OTG and VBUS_ACC pins. The reason for this is so that attached devices which support the Attach Detection Protocol (ADP) defined in OTG 2.0 can detect when they are attached to an ACA.		N/A
6.2.7	Portable Device State Diagram		N/A
	If the PD supports ACA detection, it shall continue to monitor the ID line after doing Primary detection, and respond correctly to resistance changes		N/A
6.3.1	Standard ACA Ports		N/A
	Cables can be uses to attach the Accessory Port of a Standard ACA to an accessory		N/A
	A Standard ACA Charger Port connector		N/A
	Standard ACA Connectivity Options		N/A
6.3.5	Standard ACA Requirements		N/A
	A Standard ACA Charger Port shall draw less than ISUSP when anything other than a Charging Port is attached to it.		N/A
	A Standard ACA Accessory Port shall draw less than ISUSP when a Charging Port is attached to the ACA Charger Port and nothing is attached to the OTG Port or Accessory Port.		N/A
	The resistance between VBUS_CHG, and either VBUS_OTG or VBUS_ACC of a Standard ACA shall be RACA_CHG_OTG when the Charger Switch is closed in Table 6-1, and the voltage on VBUS_CHG is at VACA_OPR.		N/A

BS EN 62680-1-1:2015			
Clause	Requirement + Test	Result - Remark	Verdict
	The resistance between the internal ground of the Standard ACA and the ground pin of a Micro-AB receptacle attached to the OTG port of an ACA shall be ROTG_ACA_GND. This requirement limits the difference between OTG and ACA ground under conditions of high charging current. This in turn allows the OTG device to reliably detect the ACA ID resistance under conditions of high charging current.		N/A
	When a Standard ACA detects VBUS_CHG asserted, it shall output VDP_SRC on DP_CHG. If the ACA detects DN_CHG greater than VDAT_REF, then it shall close its Charger Switch for as long as VBUS_CHG remains above VOTG_SESS_VLD. Note that this could result in the ACA drawing more than ICFG_MAX from a PS2 port.		N/A
	If the Charger Port was attached to a CDP, then it's possible that DN_CHG may go below VDAT_REF of the ACA due to charging currents causing the CDP ground to be lower than the ACA ground. It's also possible that the CDP could issue a USB reset. The ACA shall ignore either of these effects, and continue to leave its Charger Switch closed. When VBUS_CHG goes below VOTG_SESS_VLD, then the ACA is required to again check for VDN_CHG being greater than VDAT_REF, before opening the Charger Switch.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict

Attachment 1: Failure Voltage

4.1.5	**TABLE: Failure Voltage**						P
Ambient temperature (℃)		:		25			—
Power source for EUT: Manufacturer, model/type, output rating:				--			—
Component No.	Fault Condition	Supply voltage, (V)	Test time (min)	Output 1 (VDC)	—	—	Observation
U2 pin (1-4)	Sc	157.5/ 275	10	0.001	--	--	Unit shut down, no damage
U1 pin (1-6)	Sc	157.5/ 275	10	0.001	--	--	F1 opened immediately, unit shut down, no hazards.
USB output terminal	Sc	157.5/ 275	10	0.001	--	--	Unit shut down, no damage
E1	Sc	157.5/ 275	<1s	0	--	--	F1 opened immediately, unit shut down, no hazards.
BD1	Sc	157.5/ 275	<1s	0	--	--	F1 opened immediately, unit shut down, no hazards.
supplementary information:							
Sc=Short circuit, Oc=Open circuit							

Important

1. The test report is invalid without the official stamp of CVC;
2. Any photocopies or part photocopies of the test report are forbidden without the written permission from CVC;
3. The test report is invalid without the signatures of Approval and Reviewer;
4. The test report is invalid if altered;
5. Objections to the test report must be submitted to CVC within 15 days;
6. Generally, commission test is responsible for the tested samples only;
7. “P” means “pass” , “F” means “fail”, “N/A” or “—” means “not applicable” and “ / ”means “not test”.

*** When the CMA label is not included in the report, the test data and results will be used for research, teaching or internal quality control purposes only***

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